(12) AUSTRALIAN PATENT ABRIDGMENT
(19) AU

(11) AU-B-22536/83

0 557 723

(54) ELECTRONIC MEMORY SYSTEM

(71) BLUE CIRCLE SOUTHERN CEMENT LIMITED

(21) 22536/83 557723 (22) 17.12.82
(23) 19.12.83 (24) 17.12.82
(43) 21.6.84 (44) 8.1.87
(51)[3] G11C 5/00

(72) KEVIN JOHN BURKE

(74) SF

(57) Claim

1. A solid state memory system for emulating a rotating magnetic memory device, said memory system comprising electronic controls means adapted to be connected to a host computer, and a semi-conductor memory connected to said electronic control means, said electronic control means having circuit means for translating address signals from said host computer for the magnetic memory device to corresponding address signals for said semi-conductor memory, wherein no modifictions are required to said host computer when said solid state memory system replaces said rotating magnetic device.

55772

FORM 10

SPRUSON & FERGUSON

COMMONWEALTH OF AUSTRALIA
PATENTS ACT 1952

COMPLETE SPECIFICATION

(ORIGINAL)
FOR OFFICE USE:

Class Int. Class

22536/83.

Application Number: PF 7315
Lodged: 17th December 1982

Complete Specification Lodged:
Accepted:
Published:

Priority:
Related Art:

This document contains the amendments made under Section 49.

This is correct for printing.

Name of Applicant: BLUE CIRCLE SOUTHERN CEMENT LIMITED

Address of Applicant: 1 McLaren Street, North Sydney, New South Wales 2060, Australia

Actual Inventor(s): KEVIN JOHN BURKE

Address for Service: Spruson & Ferguson, Patent Attorneys, Level 33 St Martins Tower, 31 Market Street, Sydney, New South Wales, 2000, Australia

Complete Specification for the invention entitled:

"ELECTRONIC MEMORY SYSTEM"

The following statement is a full description of this invention, including the best method of performing it known to me/us

The present invention relates to the replacement of rotating magnetic memory (storage and controller) by a solid state mass memory sub-system. The invention is particularly, but not solely, directed to a semiconductor memory which emulates the fixed head drum memory of a computer system, such as the Foxboro Fox 2 computer system.

The standard memory for a computer system such as the Foxboro Fox 2 is a conventional rotating drum (disk) storage unit and associated controller. However, due to the electro-mechanical construction of the rotating drum/fixed head disc memory, the memory is limited in its operation. Furthermore, faults in the electromechanical unit can increase the down time and maintenance cost of the computer system.

It is an object of the present invention to overcome, or substantially ameliorate, the abovedescribed disadvantages by providing a semiconductor mass memory sub-system which emulates a rotating magnetic memory, such as the fixed head drum and drum controller used in a Fox 2-30 process control computer.

According to the present invention, there is provided a solid state memory system for emulating a rotating magnetic memory device, said memory system comprising electronic control means adapted to be connected to a host computer, and a semi-conductor memory connected to said electronic control means, said electronic control means having circuit means for translating address signals from said host computer for the magnetic memory device to

corresponding address signals for said semi-conductor memory, wherein no modifications are required to said host computer when said solid state memory system replaces said rotating memory device.

The "solid state" semiconductor memory unit of the

outages. Single bit error detection and correction logic ca also be provided on the memory boards.

Advantageously, diagnostic aids for fault location are provided through an on-board microprocessor. This microprocessor can be switched into operation when the drum emulator (DME) is not being accessed by the host system. It interfaces to the unit through the same path as the host and is thus able to test almost all the logic and memory of the system. In addition to test diagnostics, the microprocessor through a serial port, is also able to access the contents of the memory.

Notwithstanding other forms of the present invention a preferred embodiment thereof will now be described, by way of example, with reference to the accompanying drawings in which:-

Fig. 1 is a schematic block diagram of a computer system in which the present invention is applicable;

Fig. 2 is a schematic block diagram of the preferred embodiment of the mass memory sub-system of Fig. 1;

Fig. 3 is a schematic block diagram of the control board of Fig. 2;

Fig. 4 is a schematic layout of the display of Fig. 2

Fig. 5 illustrates timing cycles for the memory of Fig. 2;

Fig. 6 illustrates timing cycles for write data transfers;

Fig. 7 illustrates timing cycles for read data transfers; and

Fig. 8 illustrates read/write timing sequences.

The drum memory emulator (DME) of the preferred

present invention eliminates unreliable mechanical components; and includes the following advantages:

No rotational latency.

As the mass memory sub-system does not depend on rotating magnetic media as in the prior art, there is no waiting for information contained on part of the disc (drum) to reach the heads.

Increased storage capability.

The mass memory sub-system typically can store up to a nominal four megabytes of data compared with the storage capacity of a nominal two megabytes of the drum memory sub-system it replaces.

Increased transfer speed.

The transfer speed of the mass memory sub-system is increased since it is not limited by the speed of the rotating disc. The transfer speed is also variable.

Little inter-group delay.

The known drum and drum controller transfer four words at a time with a gap in between each group. The minimum transfer that the system can support is sixteen words. In contrast, the mass memory sub-system can communicate with a processor in groups of a variable number of words with a very small delay in between groups.

Increased relability.

Since the mass memory sub-system is completely electronic, it is not subject to the vagaries of the electromechanical drum sub-system as far as mechanical reliability is concerned.

Preferably, the memory contents are kept secure through the provision of battery back-up during power

embodiment comprises the following components:

(1) Control board.

(2) Four memory boards.

(3) System housing and back plane.

(4) Power supplies, standby battery, and display panel.

The function of the control board is the decoding, by hardware, of an address expressed by the host computer system as a number of blocks (to be transferred) and starting track and block. Fig. 3 illustrates the major data paths used within the control board circuit. The size of the transfer and the starting address are decoded by hardware to the module group and address, and the number of words in the mass memory sub-system. Parity is generated or read by logic 60 contained on the control board as the transfer proceeds. Refreshing of dynamic RAMs on the memory boards is continued while a transfer is being made from the mass memory sub-system to the host system. Logic on the control board allows adjustable numbers of words per group, adjustable delay between blocks and the emulation of the appropriate control signals that the original drum memory sub-system produced.

Also contained on the control board is a microprocessor 50 complete with its own read/write memory and programmable read only memory. This microprocessor can communicate with an external standard computer terminal. By emulating the functions of the host system, the microprocessor allows the testing of practically all the electronics contained in the sub-system. The microprocessor also allows the user to examine or modify the mass memory

sub-system's memory. Simultaneous access to the mass memory sub-system's memory is not permitted. A sixteen byte bi-directional port is provided on the control board. This port will permit high speed transfer to back up devices, for example, in further embodiments of the mass memory sub-system.

As can be seen from Fig. 3, the microprocessor's point of access to the memory unit is effectively in parallel with the host computer interface from the data bus interface (DBI). This means that virtually all control in data paths are capable of being tested by the microprocessor. A switch on the inside of the display panel 40 at the front of the unit controls whether the microprocessor or host have access to the memory.

The microprocessor, DBI interface, memory refresh and control logic are all accommodated on a single printed circuit board called the drum memory controller (DMC). The DMC is plugged into a back plane of a housing from which it derives its power. The housing is preferably of alumninium construction and physically compatible with the original drum memory. The back plane distributes signals from the DMC to each of the memory boards (DRB) and to the DBI connector. Each memory board stores 512K sixteen bit words.

The front edge of the DMC has connectors from which signals are sent via ribbon cable to the display board 40 mounted behind the front door of the system housing. An RS 232 interface and a parallel port are also provided on the DMC. The RS 232 port is for connection to a terminal if it is desired to operate the on-board microprocessor.

A display 40 on the front panel of the system displays most operational aspects of the unit. It is

INIT	Memory being Initialized by Microprocess
DIAG	Diagnostic Test Running
MON	Debug Monitor in Use
ACTIVE	Microprocessor Operational but not in Us

In addition to front panel indicators, the system memory boards have status indicators as follows:-

SELECT	GREEN LED	Memory PCB Selected
MERR	RED LED	Multi-Bit Error Detected
EDC	RED LED	Single Bit Error Detected and Corrected
FAULT	YELLOW LEDS	Five Bit Fault Code
GROUP	YELLOW LEDS	Three Bit Bank Select Code

DESCRIPTION OF OPERATION

The system logic consists of two main sections - the drum memory control board (DMC) and the memory boards (DRB). The DMC provides all interface logic between the host system's DBI and the memory boards. Up to 4 512K word memory boards can be driven by the DMC. All boards communicate via a printed circuit backplane.

MEMORY BOARD

Each memory board provides 512K words of read/write storage using 64K bit dynamic RAM integrated circuits. The memory is arranged as an array of 168 of these ICs giving a 512K x 16 bit memory with 5 additional parity bits.

The five parity bits are used to allow the board to detect and correct single bit data errors and detect most multi-bit errors. The single bit error detection and correction allows the board to operate normally through single memory IC failure or the more likely "soft" error

arranged so as to provide similar information to the original drum storage system plus that information peculiar to this unit. The format of the displayed data is designed to show the correlation between the original drum and the new Mass Memory system. This is done by the grouping and by dual labels on the display, as shown in Fig. 4.

All indicators are red LEDs. The functions of these are as follows:

TRACK	Drum Track Address
BLOCK	Block Address (242 blocks per track)
WORD	Word Number within Block (16 words per block)
MODULE	Memory Module (UP TO 4)
GROUP	64K Word Group on each PCB (8 per PCB)
ADDRESS	Address within 64K Group
CORE LOCATION	CPU DMA Address
NUMBER OF BLOCKS	Number of Blocks to be Transferred
WRITE	CPU to Memory System Write in Progress
READ	Memory System to CPU Read in Progress
INT	Memory System Interrupt Pending
DTC	Drum Transfer Complete
P.E.	Memory System Multi-Bit Error Detected
D.O.E.	Drum Overflow Error (attempted access beyond available drum system memory)
C.O.E.	Core Overflow Error (attempted transfer beyond available CPU memory)
ON-LINE	Host CPU has Access to Memory
STANDBY	Main Power has Failed and Unit is on Battery Power

The signals from the backplane are used by the memory boards to determine the operation to be performed. The board select signals BSEL2-3 are set up by the DMC and are compared to an on-board jumper selectable address. If the address set up on the jumpers matches the binary code on the BSEL2-3 lines, then the board is selected and is ready for memory transfers. (The green "SELECT" LED on the PCB will illuminate if the board is selected). Note that each board should have a unique address set up on the DIL switches to avoid conflict on the backplane.

At the start of a memory cycle, the read/write line MWRITE- and the address lines MUXA0-6 will be set up by the DMC. The low order 7 bits of the address are formed from the Word Address (WA0-WA3) and Block Address bits (BA0-BA2) put on MUXAO-6 by the DMC and are buffered from the backplane and presented to the memory array. The eighth multiplex address line is generated on board by an IC which multiplexes it from the GRPO-1 lines which are the two most significant address lines needed to address 64K. Each bank of memory ICs has its own buffer. Each buffered address line drives the memory ICs associated with it via a small resistor to minimise ringing and overshoot.

After the low order address is set up, the signal BRAS- is asserted. This signal is also buffered and drives all ICs of the memory array. Next the high order address is set up on the MUXAO-6 lines and the signal BCAS- is asserted. The high order seven bits are formed from remaining Block Address bits (BA3-BA7) and the least significant two bits of the Track Address (TA0-TA1).

The above addressing technique is used to access

occurring due to the effect of ALPHA particle radiation on an individual IC.

Dynamic RAM ICs such as the ones used in the design, employ a system of multiplexed address lines to allow them to be housed in a small package. With the (type 4164) 16K x 1 bit used, 16 bits of address are necessary to access each cell of the 65536 available. This address is presented as two lots of 8 bits. The low order 8 bits are strobed into the IC by a ROW ADDRESS STROBE (RAS) followed by the high order 8 bits using a COLUMN ADDRESS STROBE (CAS).

The memory board design uses this multiplexing technique for its operation, with these signals being generated on the control board.

The signals presented to the memory boards from the backplane are as follows:-

TABLE 1: SIGNAL LIST

SIGNAL	FUNCTION
MD0-MD15	BI-DIRECTIONAL DATA BUS
PARITY	BI-DIRECTIONAL PARITY BIT (ODD)
MUXA0-6	MULTIPLEXED ADDRESS BUS
GRP0-2	MEMORY GROUP SELECT (WITHIN A BOARD)
BSEL0-3	BOARD (MODULE) SELECT
MWRITE-	MEMORY WRITE CYCLE
BRAS-	MEMORY ROW ADDRESS STROBE
BCAS-	MEMORY COLUMN ADDRESS STROBE
PERR-	PARITY ERROR DETECTED PULSE
PAREST-	PARITY ERROR RESET PULSE
+ 5V	POWER SUPPLY
GND	

1	1	0	0	1	Multiple bit error
1	1	0	1	0	Error in data bit 5
1	1	0	1	1	Multiple bit error
1	1	1	0	0	Error in data bit 15
1	1	1	0	1	Multiple bit error
1	1	1	1	0	Multiple bit error
1	1	1	1	1	Multiple bit error

With the information derived from this fault code it is possible to correct the bit in error and flag that this has occurred.

The basis of the ECC circuit is five 74S280 9-bit parity generators. These are used in two modes determined b a signal BWR-. When BWR- is low, the ninth input to the 74S280s goes low and they become 8 bit parity generators use to generate the five check bits written into memory during a write operation. If BWR- is high then the check bits from the RAM are gated to the ninth input of the 74S280s which produces the fault code.

If there is a single bit error then the fault code i used to correct the data bit in error. This is done by grouping the five fault code bits with four data bits to for the address input of a PROM. When no fault is detected the codes stored in the PROM produce a data output corresponding to the four data bits on the address lines. If an error is detected which affects any of the four data bits in a particular PROM then the data pattern output is the correcte version of the data on the address inputs.

Using the PROM, error correction becomes a function of selecting a "table" of codes in the PROM with the appropriate bit reversed from normal.

following table.

FAULT CODE					ERROR
F0	F1	F2	F3	F4	
0	0	0	0	0	No error detected
0	0	0	0	1	Error in check bit 4
0	0	0	1	0	Error in check bit 3
0	0	0	1	1	Error in data bit 0
0	0	1	0	0	Error in check bit 2
0	0	1	0	1	Error in data bit 1
0	0	1	1	0	Multiple bit error
0	0	1	1	1	Error in data bit 3
0	1	0	0	0	Error in check bit 1
0	1	0	0	1	Error in data bit 4
0	1	0	1	0	All data and parity set to logic 1
0	1	0	1	1	Error in data bit 6
0	1	1	0	0	Error in data bit 7
0	1	1	0	1	Error in data bit 8
0	1	1	1	0	Error in data bit 9
0	1	1	1	1	Multiple bit error
1	0	0	0	0	Error in check bit 0
1	0	0	0	1	Error in data bit 11
1	0	0	1	0	Error in data bit 12
1	0	0	1	1	Error in data bit 13
1	0	1	0	0	Error in data bit 14
1	0	1	0	1	All data and parity set to logic 0
1	0	1	1	0	Error in data bit 2
1	0	1	1	1	Multiple bit error
1	1	0	0	0	Error in data bit 10

locations within any 64K group of memory. The 64K group and board to be accessed is determined by the higher order TRACK ADDRESS line TA4-TA8. TA2-TA4 are buffered to form GRPO-2 and drive the backplane bus. They are used by each memory board to select one of the eight 64K groups of memory. TA5-TA8 are also buffered to form BSEL0-3 which determines the board selected on the backplane.

When a board is selected, an IC will decode the GRPO-2 lines to determine which memory group will receive the Column Address Strobe (CAS-). The output from the decoder generates eight CAS signals, each of which is passed through a 33-47 ohm resistor to drive the groups of associated memory ICs.

If the operation being performed is a write to memory (MWRITE- low), the data on the backplane MDO-15 is buffered to generate the internal data bus DO-D15 and presented to the memory array via buffers.

From the internal data bus 32 the parity generators 60 generate a five bit code (WPO-WP4) which is sent to the data input lines of five parity RAMs, to be stored at the same time as the data.

During a read operation, the data read from the memory array is buffered and drives the internal data bus D0-D15. This time the outputs of the five parity generators are compared to the five bits of data read from the parity RAMs and a fault code F0-F4 generated. This fault code is compared with the data D0-D15 in ROMs to "recreate" the data which is then buffered and presented to the DMC on the backplane.

The dynamic RAMs used in this design require periodic

refresh to maintain memory contents. Refresh is performed on all boards simultaneiously by the DMC. This is carried out by performing a RAS only memory cycle. In this way, all boards are refreshed independently of the "select" condition. Each refresh cycle is generated with the MWRITE- line high, and the MUXAO-6 lines cycling through all possible combinations. Figure 5 gives the timing expected on the memory board.

Error Checking and Correcting (ECC)

The ECC used on the memory boards is based on Hamming codes. The procedure involves splitting the data word into five groups and generating a parity bit for each. Each group is made up of 8 bits chosen from the 16 bit data word. The five check bits and the data bits from which they are generated are shown below.

CHECK BIT	DATA BITS
0	2 5 10 11 12 13 14 15
1	4 5 6 7 8 9 10 15
2	1 2 3 7 8 9 14 15
3	0 2 3 5 6 9 12 13
4	0 1 3 4 6 8 11 13

During a memory write operation the five check bits are stored into RAM at the same as the sixteen data bits. When the data is read from RAM the 16 bit word is retrieved, from which the five parity bits are again generated. This time the five parity bits are compared to the five previously stored in memory, on a bit by bit basis. If a difference is found then a "one" is generated in a five bit fault code corresponding to this difference and the fault code formed indicates the type of error detected and is shown in the

If either of the two RED LEDs (EDC or MERR) are illuminated then a fault has occurred on the memory board. In this case the YELLOW LEDs will be fixed in a pattern representing the source of the fault. Using these LEDs and the preceding tables it is possible to trace the fault to a particular memory IC.

The YELLOW LEDs indicate the PARITY CODE written int memory during a write operation, so that these and the BANK LEDs will be active. During a read the FAULT CODE LEDs will all be off (so long as no fault occurs) and the BANK LEDs will be active.

DATA OUTPUT BUS

A Data Output bus (DATO) 10 from the DBI interfaces to the DMC through tri-state buffers. The signals from the DBI are enabled onto an internal data output bus 15 if the system is ON-LINE. The signals are taken to all registers within the DMC which are loaded from the CPU and the latches used to hold data for transfer to DME memory.

The internal data output bus 15 can alternatively be driven by the outputs of other latches 52 if the microprocessor 50 has access. The microprocessor must load the two eight-bit latches from its bus independently by generating outputs forming the 16 bit word needed for commands and data.

DATA INPUT BUS

A Data Input bus 12 to the DBI is driven by buffers 13 from the internal data input bus 32. The buffers 13 are only enabled when the DME and DBI are transferring data during a DMA read.

The internal bus is generated from the outputs of tw

The five bit fault code is used by itself to address a fifth PROM. This fifth PROM has two functions. The first of these is to produce an indication if an error occurs and the second is to supply a code to assist fault finding. A fault indication is given if either a multiple error occurs or a single bit error is corrected. If the "Error Detected and Corrected" LED comes on, the system will continue operation but it is advisable that the faulty chip is found to avoid a multiple error. If the "Multiple Bit Error" LED comes on, a PARITY ERROR will be signalled to the computer and the transfer terminated.

FAULT ISOLATION

The memory board has a number of LEDs which indicate the operation being performed. Typically the LEDs are arranged in a row as follows:

GREEN	- Board selected
RED	- Multiple bit error detected (MERR)
RED	- Single bit error detected and corrected (EDC)
YELLOW	- F0 Fault (Parity code)
YELLOW	- F1
YELLOW	- F2
YELLOW	- F3
YELLOW	- F4
YELLOW	- B2 Bank selected
YELLOW	- B1
YELLOW	- B0

eight-bit latches 33 which hold data words read from the DME memory. The information on the internal bus can be read at any time by the microprocessor 50, onto its data bus, through tri-state buffers 51. Note that the Data Input bus 12 to the DBI can also be driven independently by a buffer which enables the status information onto the bus in response to a STATUS read command.

ADDRESS BUS

An Address Bus 14 to the DBI is driven by integrated circuits 16 which buffer the contents of a core location counter 38. These lines have termination resistor networks to help eliminate ringing and crosstalk and are formed from a 180 ohm resistor to +5V and a 390 ohm resistor to ground.

CORE LOCATION COUNTER (CLC)

The Core Location Counter 38 is a set of four-bit parallel load counters. These counters are loaded during transfer initialization from the internal data output bus 15. The respective outputs of the counters are buffered to indicate to the CPU the memory location to be accessed during a DMA transfer. The counter is incremented at the end of each DMA CPU memory cycle.

BLOCK ADDRESS REGISTER (BAR)

This register/counter 36 is formed from two four-bit parallel load counters which are loaded from data output bus 15 during a transfer initialization sequence. The output of the counters form Block Address signals BA0-BA7. Advantageously, the counters are modified so as to be module 242 counters by additional ICs which force a reset to both counters at count 242. In this manner, the system simulates the number of blocks the original drum had per track. The

Block Address is incremented at the end of each sixteen word block transferred. When the Block Address counter is at count 241, the next block transferred will generate a pulse to increment the Track Address.

TRACK ADDRESS REGISTER (TAR)

This register/counter 36 is formed by a counter which is loaded from the internal data output bus 15. The counter outputs TA0-TA8 represent the pseudo drum track selected. This register is incremented at the end of each track (242 blocks).

WORD ADDRESS COUNTER

A four-bit counter 39 (outputs WA0-WA3) is used to indicate the current word within a block being accessed. After every sixteen words (one block) a carry output generates a signal which is used to increment the Block Address Register 36 and the Number of Blocks Register 35.

NUMBER OF BLOCKS REGISTER (NBR)

This register 35 is formed by counters which are loaded by a pulse generated during the transfer initialization sequence. The outputs are used to drive the front panel indicators and give the number of blocks still to be transferred. This register controls the size of the transfer to be made and must be a minimum of one block.

After this register is loaded it is automatically decremented by one. From then on, as each block is transferred, it is decremented by a pulse. When the counter is at zero then the pulse received will cause a signal to be generated from a "BORROW" output of the counter to signal completion of a transfer.

Patent Abstracts of Japan

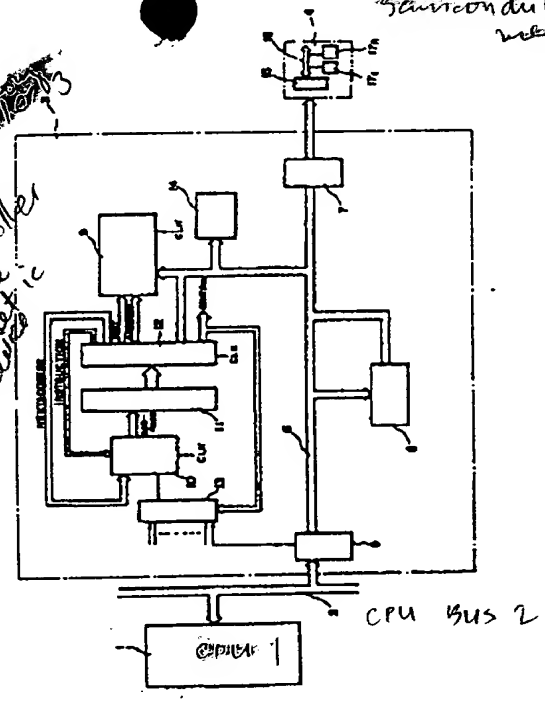
PUBLICATION NUMBER : JP60178564
PUBLICATION DATE : 12-09-85
APPLICATION NUMBER : JP840033801
APPLICATION DATE : 24-02-84

VOL: 10 NO: 30 (P - 426)
AB. DATE : 05-02-1986 PAT: A 60178564
PATENTEE : MEIDENSHA KK
PATENT DATE: 12-09-1985

INVENTOR : SHINOZAKI MICHIO

INT.CL. : G06F13/16; G06F3/06;
G06F12/02

TITLE : AUXILIARY STORAGE DEVICE



ABSTRACT : PURPOSE:To improve a data transfer speed by using a semiconductor memory as a storage element, and allowing information transfer from a computer in the same access mode with the mode of access to a magnetic disk device.
CONSTITUTION:A central processing unit 1 is coupled with a main controller as the interface of a semiconductor disk device through a CPU bus 2, and information is transferred to and from the semiconductor memory unit 4 under the control of the memory controller 3. The central processing unit 1 is allowed to transfer information to and from the controller 2 in the same access mode with a magnetic disk, and the controller 3 performs processing required to write and read the information to and from the semiconductor memory unit 4 while processing necessary for the magnetic disk is omitted. The controller 3 emulates the controller of the magnetic disk device.

3. CORE MEMORY STARTING ADDRESS - core address at which to start transfer.

4. SIZE OF TRANSFER - number of data blocks to be transferred.

5. COMMAND TO START THE TRANSFER.

These steps are performed by a sequence of four instructions (command words) issued to the mass memory control unit (DMC). Each instruction causes an IOT pulse to be generated in the DBI. Each of the IOT pulses are buffered by "hysteresis - input" inverters 11 on the DMC before being used. They also have a pull-up resistor and capacitor to aid in the removal of induced noise.

The instructions have the following order and format

First Instruction (IOT 1): This instruction loads a first drum control register to clear the address/control registers and error flags.

Second Instruction (IOT 2): This instruction loads second drum control register with the MSB of the starting block address and the starting core location.

Third Instruction (IOT 3): This instruction loads a third drum control register with the remaining low order bit of the block address and the starting track register.

Fourth Instruction (IOT 4): This instruction is a load to the first drum control register with the number of blocks to be transferred, the Read/Write direction bit and a GO bit. This instruction generates an IOT 1 pulse and behaves as the first instruction. However, this instruction is the one which loads the number of blocks counter 35 and starts the transfer.

Note that the signals used for loading/clearing

DISPLAY INTERFACE

The front panel display 40 of the DME is driven from the DMC and gives a visual indication of many of the DMC's registers as well as its operating mode and status. The signals to the display are provided by the DMC on two ribbon cable headers.

SYSTEM INTERFACE

The interface of the mass memory of the preferred embodiment to the FOX 2/30 system is via the Data Bus Interface module (DBI). Through the DBI, the CPU is able to set up transfers to the mass memory system by loading registers for the size, direction and the starting location (in CPU memory and mass memory) of the transfer. These set up procedures in the software of the CPU need not be modified for this system as the DME emulates the original drum controller's registers completely.

During normal operation, reading or writing of the drum is controlled and executed by a "System Librarian" and other programmes of the FOX 2/30 operating system. Programming instructions issued by the processor to initialize and/or control the drum are executed through the DBI.

When a programme requires a data transfer between the mass memory unit and core memory, the processor enters a service routine to initialize the mass memory unit. This initializing transmits the following information to the mass memory:-

1. TRANSFER DIRECTION - read or write.
2. STARTING ADDRESS - track and block at which to start transfer.

registers above can be generated by the microprocessor 50 independently and are OR'ed with the CPU generated signals. When the DMC is ON-LINE the microprocessor is still capable of generating these signals although its program should not allow this.

Once a drum transfer has been initiated, the drum controller will transfer data to/from CPU memory via direct memory access. The transfer takes place without programme intervention but the programme is able to determine when the transfer is complete by examining a Status register. This register is cleared when the first instruction (IOT 1) is issued above, and has bits indicating the reason for transfer termination. This register can be read at any time.

INTERFACE SIGNALS

The interface from the DME system to the FOX2 computer is via the DBI. The DBI has a connector plate from which all interface signals are distributed to the control system. The original Drum Memory Sub-system uses a 75 Pin WINCHESTER style connector. A two metre cable assembly is normally provided between this and a Drum Control Module (DCM) and mates with a connector (on the DCM) using the same style of connector as above.

The DME system is designed to use this existing cable assembly and provides a 75 pin MALE WINCHESTER connector for this purpose at the rear of the unit. This connector is mounted on the PCB backplane assembly and signals from it are sent to DMC.

The signals used by the DME consist of sixteen data lines for the output of data and commands to the DMC; sixteen data lines for the input of data and status

information from the DMC; fifteen address lines generated by the DMC for use by the CPU during DMA transfers to indicate current memory address and twelve control lines are also present.

WRITE DATA TRANSFER

Timing for write data transfers is shown in Fig. 6. When the transfer direction is specified as a write to the DME, then on instruction IOT 4, a first flip-flop will be set, and a SETGO- pulse will be generated. This pulse will set a DMA REQUEST flip-flop (DMARQ-), thus asserting a line to the DBI via a buffer.

A GO flip-flop is set by the SETGO- pulse and is used to indicate to the DBI via a buffer that the DMC is busy in transfer (STATUS). GO also causes the indicator "WRITE" to be illuminated on the front display panel 40.

In response to the DMA request, the DBI generates a MASTERL pulse. This pulse is synchronised with a CPU memory cycle and is used to indicate timing for the DME memory transfer. The MASTERL pulse is received and buffered. This signal can be quite noisy and is cleaned up by a monostable and flip-flop to provide a MASTER+ pulse. A one-shot triggers and generates a 400 nSec pulse to eliminate leading edge noise and a monostable triggers and generates a 150 nSec pulse to remove noise at the trailing edge of MASTERL.

After the first MASTER pulse is received, MQ2- is generated and sets a second flip-flop (active write). This operation prepares the "D" input of a memory cycle flip-flop to allow memory cycles on subsequent MQ1- pulses. (This pulse occurs during the first part of a MASTER pulse and the above sequence is designed to delay memory cycles until afte

the first MQ1-.) The trailing edge of the first MASTER pulse is used to latch the data just read from the CPU memory. It also advances a core location counter 38 in preparation for the next CPU memory cycle.

When the second (and any subsequent) MASTERL pulse is received, MQ1 is generated. The trailing edge of this pulse clocks the memory cycle flip-flop. Its "D" input will be low from the first MASTER pulse and MEM+ (MEM-) will be set true.

The memory cycle thus initiated writes the data (stored in latches 37 at the end of the previous MASTER pulse) into the DME memory. At the end of this memory cycle, a pulse occurs on the timing level signal which resets the MEM flip-flop, ready for the next transfer. Thus the data read from CPU memory during one MASTER pulse is transferred to DME memory during the next MASTER pulse.

During the DME memory cycle, a timing pulse (WDCL-) is generated and is used to advance a Word Counter 39. The Word Counter outputs are used to adjust the number of consecutive CPU memory cycles which are performed without allowing the CPU to execute. This can be four or eight. (The DME is capable of reading or writing continuously to the CPU memory during a transfer but locks out the CPU while this was happening.) In real time systems it is necessary to allow some processing to be performed during a transfer and a one-shot is set to give approximately a 15 microsec gap between transfer bursts. This gap is adjustable from approximately 3 to 15 microsec if it is desired to increase transfer speed, or optimise the interrupt servicing during mass memory transfers.

If a four-word transfer were selected, for example,

then switch 5 of an 8 pole DIL switch would be closed and th Word Counter output would be connected to the input of an IC. On receipt of the fourth WDCL- pulse the Word Counter output would make a high to low transition which after being inverted by the IC and setting the second flip-flop, resets DMARQL upon receipt of the next MQ1- and MASTER pulses.

The DME memory cycle occurring from this last MASTER pulse will trigger a one-shot. When this one-shot times out (nominally 15 microSec), a 50nS pulse is generated to set th DMARQ flip-flop to initiate further DMA transfers and resets the second flip-flop.

It can be seen that the first DMA transfer burst after a write to the DME is started will cause DMARQ to be held for five MASTER pulses and all succeeding ones for four. During the transfer of the second last word of the last group, the GO flip-flop will be reset. No further DME memory cycles will occur but the DMARQ will remain asserted until the last MASTER pulse is received. Thus the last CPU memory cycle will only be a dummy operation and the data rea from CPU memory will be unused.

READ DATA TIMING

Timing cycles for read data transfers are shown in Fig. 7. If the transfer direction designated in the fourth instruction (IOT 4) is a read from DME to the CPU then the first flip-flop will be reset, and an indication sent to the DBI that a write to CPU memory is required.

The SETGO- pulse sets the DMARQ flip-flop asserting DMARQL to the DBI. It is also used to set the second flip-flop F.F. and clocks a third flip-flop. This flip-flop is set and forces the memory cycle flip-flop to be set. The

sequences will then also stop after TLG (not shown).

REFRESH TIMING

A memory refresh is performed by sequentially accessing all possible combinations of the ROW address at least once every 2 mSec. This access can be a RAS only cycle. In this system a 10 mHz clock is divided to form a 5mHz clock which drives a "COUNT UP" input of a four bit counter. As long as the DMC is not involved in a DMA transfer, then the "CARRY OUTPUT" of this counter will generate a 100nS pulse every 3.2 mSec. This pulse increment the refresh address counter and sets the refresh flip flop (REF F.F).

This REF F.F. being set causes a timing sequence described above (Fig. 8) to begin and enables the Refresh Address onto the MUXA0-6 lines. An RAS is generated at TLA and reset at TLF but no CAS occurs. The REF F.F. is reset at TLG in readiness for another cycle.

With the above arrangement, a full refresh sequence is carried out in approximately 400 microSec. Note however that during DMA transfers no refresh occurs. Thus during a sixteen word transfer, with the interblock delay set to 15 microSec, the refresh time increases to 1.25 mSec.

MICROPROCESSOR

The microprocessor 50 in the DME system is primarily designed to allow the memory and electronics of the unit to be checked out independently of a host CPU. In addition it allows a user access to the DME's memory contents for modification or examination.

The microprocessor is typically a general purpose eight bit machine with an 8K addressing range, an 8 bit data

resetting it and also clocks an INTERRUPT flip-flop.

READ/WRITE CYCLE TIMING

When either a read or write memory cycle is to occur, then MEM+ is set. When it is set, then a seven phase timing sequence is started. This sequence is illustrated in Fig. 8.

At the start of a memory cycle, the address lines would have been stable for some time (a first multiplexer selects the Row Address lines) and so it is possible to generate the RAS to memory. This is done with TLA- setting a flip-flop which is buffered to form the BRAS- signal to the memory boards.

100 nS later at TLB, a flip-flop is set, which switches the first multiplexer to enable the Column Address to the memory boards.

At TLC, CAS flip-flop is set. CAS- is buffered to drive the memory boards with BCAS-.

The memory is now addressed and at TLD the WORD CLOCK WDCL- is generated to advance the memory address, formed from WORD, BLOCK and TRACK counters, ready for the next memory cycle.

If the memory cycle was a READ operation, then at the trailing edge of TLE the data will be ready and an IC generates RDATAN- which is used to latch the data from the memory into latches.

If the memory cycle was a WRITE operation, then a signal MWRITE- would have been generated to indicate to the memory boards that a write is to occur and to enable the data stored in latches onto the data bus to the memory boards.

Either cycle is completed when TLF resets the RAS and CAS flip-flops and associated logic. The timing pulse

setting of the memory cycle flip-flop will be delayed briefly however, if a memory refresh cycle happens to be in progress. The data from the DME memory boards is valid during a predetermined timing level of the cycle.

The data for the first CPU memory write is thus ready and when the first MASTER pulse is received it is enabled onto the DATA INPUT bus 32 for use by the CPU. The MASTER pulse generates MQ1-, the trailing edge of which is used to clock the MEM+ flip-flop so as to initiate another DME memory read.

Thus the data for transfer to the CPU is read from DME memory during the previous MASTER pulse.

As with the write transfer, described above, each DME memory cycle causes the Word Counter 39 to be advanced. After every four (optionally eight) memory cycles, the second flip-flop is set and DMARQL cleared on the following MASTER pulse.

TRANSFER TERMINATION

Once a DME transfer is initiated, it can be terminated in the following ways:

OPERATION	REASON FOR TERMINATION
Read/Write	Drum Transfer Complete (DTC)
Read/Write	Core Overflow Error (COE)
Read/Write	Drum Overflow Error (DOE)
Read Only	Parity Error (PE)
Read/Write	Drum Timing Error (DTE)
Read/Write	System Off-Line/Standby (SOL)

All the conditions above, except SOL, act in the same fashion. They each set a flip-flop which is read as part of the DME status word and also reset the GO flip-flop to stop

any transfer in operation. If the system is OFF-LINE or on STANDBY then no transfer will be initiated.

The above conditions are generated as follows:-

DTC is generated by a signal which results when the Number of Blocks Counter 35 counts through zero. This is the normal end of a transfer.

COE is set when a MASTER pulse is received which attempts to advance the core location counter 38 beyond the available CPU memory.

DOE is set when a DME memory cycle occurs which attempts to advance the Track Address Register 36 beyond the limit preset in DIL switches.

PE is set when a DME memory read cycle operation is performed and a parity error exists on the data received from the memory board.

DTE is set when a timeout occurs during a DMA transfer i.e. no MASTER pulse is received within 10 microSec of DMARQ being asserted. A retriggerable monostable is triggered when DMARQ is first asserted (MQ1- is high) and on the receipt of each MASTER pulse (MQ1- pulses and DMARQ- is low). If the MASTER pulse is not received within the timeout period, a 5 microSec pulse resets DMARQ and sets a DTE flip-flop

SOL is set when an attempt is made to initiate a transfer when DME is OFF-LINE, or the system is on battery power (STANDBY). The standby signal is delayed to prevent the CPU accessing the DME for a short time after power-up.

When any of the above flip-flops are set, then a pulse (STOP+) is generated which clocks the GO flip-flop

"INIT" LED will flash continuously.)

4) A read/write check of the RAM is then performed. (If an error is found, then the "DIAG" LED will flash continuously.)

5) A read/write check of the ACIA is performed. (An error will cause the "MON" LED to flash.)

6) A read/write test of the PIA is then performed. (Any error will cause the "ACTIVE" LED to flash.)

7) If all above tests are carried out successfully, then all four LEDs are flashed briefly and the microprocessor will carry on with its internal initialization.

After all above tests are successfully concluded, then an identification message will be output via the RS232 port to the attached terminal.

Monitor Operation

When power is first applied, the microprocessor identifies itself to the user with a short message to the terminal.

At this point the microprocessor is in the "debug monitor", waiting for a command. The "monitor" programme allows the operator to access the microprocessor's memory and peripherals for test purposes.

Diagnostic Test

All pre-programmed diagnostic tests are initiated from the "diagnostic" mode. This mode is entered after the appropriate command is given from the "monitor" mode.

When this mode is entered, a short identification message is output, which gives the test operations

bus and operates with a 1MHz clock.

Control of the microprocessor is through an asynchronous serial (RS232) port provided on the board. Any simple full duplex terminal operating at 1200/9600 baud can be used. In addition, a 16 bit di-directional parallel TTL interface is provided for future use.

When the DME is in operation, only the microprocessor or the host CPU have access to the memory. Both share common data and control paths and simultaneous access is not accommodated. A switch on the front display panel 40 is used to determine which has access. If the CPU has control then the ON-LINE indicator will be illuminated.

The microprocessor also has control over four LED indicators on the front panel. These are used in one instance for the internal self-test feature and during normal operation as status indicators.

Microprocessor Self Test

On power up, the microprocessor performs an internal self-check to verify the correct operation of its EPROM, RAM and I/O interfaces. Internal self-test is of course limited, as it relies on correct operation of the microprocessor, and it cannot check out all interfaces over which it has control.

The tests performed and the sequence of indicators are typically as follows:-

1) POWER UP- all four "STATUS" LEDs on the display panels are turned on by a hardware reset signal.

2) When the microprocessor begins execution, it first of all clears all four LED's.

3) An EPROM check sum validation is then performed. (If an error is detected, then the

available. It then asks for the test parameters required which set the range over which the tests are to run. The test is then chosen from a menu. When a test has been selected, the operator is prompted to verify the choice before continuing. If a RETURN is pressed, then the test is performed once and the menu is offered again for a new selection. If a "C" is pressed, then the test will continue indefinitely.

If any errors are detected during testing, then a message will be printed giving the test location and reason for the error.

DC POWER SUPPLY

The DME system is designed to operate from a 110VAC source.

The power supply module has three distinct sections:-

1) +24VDC to +5VDC Converter

2) 110VAC to 24VDC nominal

3) Voltage Monitor and Sequencer

The converter is preferably based on a three terminal switching regulator. These units not only provide the required voltage conversion but do it at high efficiency and over a large input voltage range. The output is run to the sub-system I/O connector and to the respective test points and LED indicators on the panel. Note that the high currents used by the DME on the +5VDC line necessitate the use of remote voltage sensing to sense losses on the power cabling.

The Power Supply Monitor section in the unit provides two main functions. Firstly, it incorporates circuitry to sense over-voltage on the 5VDC. (If the supply does exceed its nominal rating by more than approximately 1V then an SCR

"crowbar" is switched on to shunt that output.) Secondly, this module provides power switching circuitry which ensures that the +5V supply to the unit is maintained from batteries when the AC supply fails.

The power supply sub-system presents a very heavy capacitive load to the +24V source at initial power up, and special precautions should be taken to ensure that the +24V ON-OFF switch will operate correctly. The surge current is limited by a transistor switch which is activated by the front panel toggle switch.

Since the DME system is operated with a host system powered from 110VAC, a power supply is provided to convert from this to the +24VDC used. This power supply is internal to the DME. The 24V load is approximately 2.1 Amps.

This power unit also incorporates a simple scheme to trickle charge the 24V batteries used to maintain system power during mains outages.

The unit operates by generating an unregulated 24VDC (normally around 30V) with a simple bridge rectifier and capacitor from a transformer. This becomes the 24V source to the DME via a blocking diode. A small current is able to pass from the supply to the battery (approximately 100 mA).

When AC power fails, a power transistor is switched on, which allows the 24VDC to be supplied from the battery. Another transistor is used (with a zener reference) to signal the AC failed condition (STANDBY) to the DME.

The foregoing describes only one embodiment of the present invention, and modifications obvious to those skilled in the art can be made thereto without departing from the scope of the invention. For example, although the drum

memory emulator has been described with reference to a Foxboro Fox 2 computer, it can be modified to suit other computer systems. Thus, the present invention can be used to emulate a moving head disk memory device.

The claims defining the invention are as follows:-

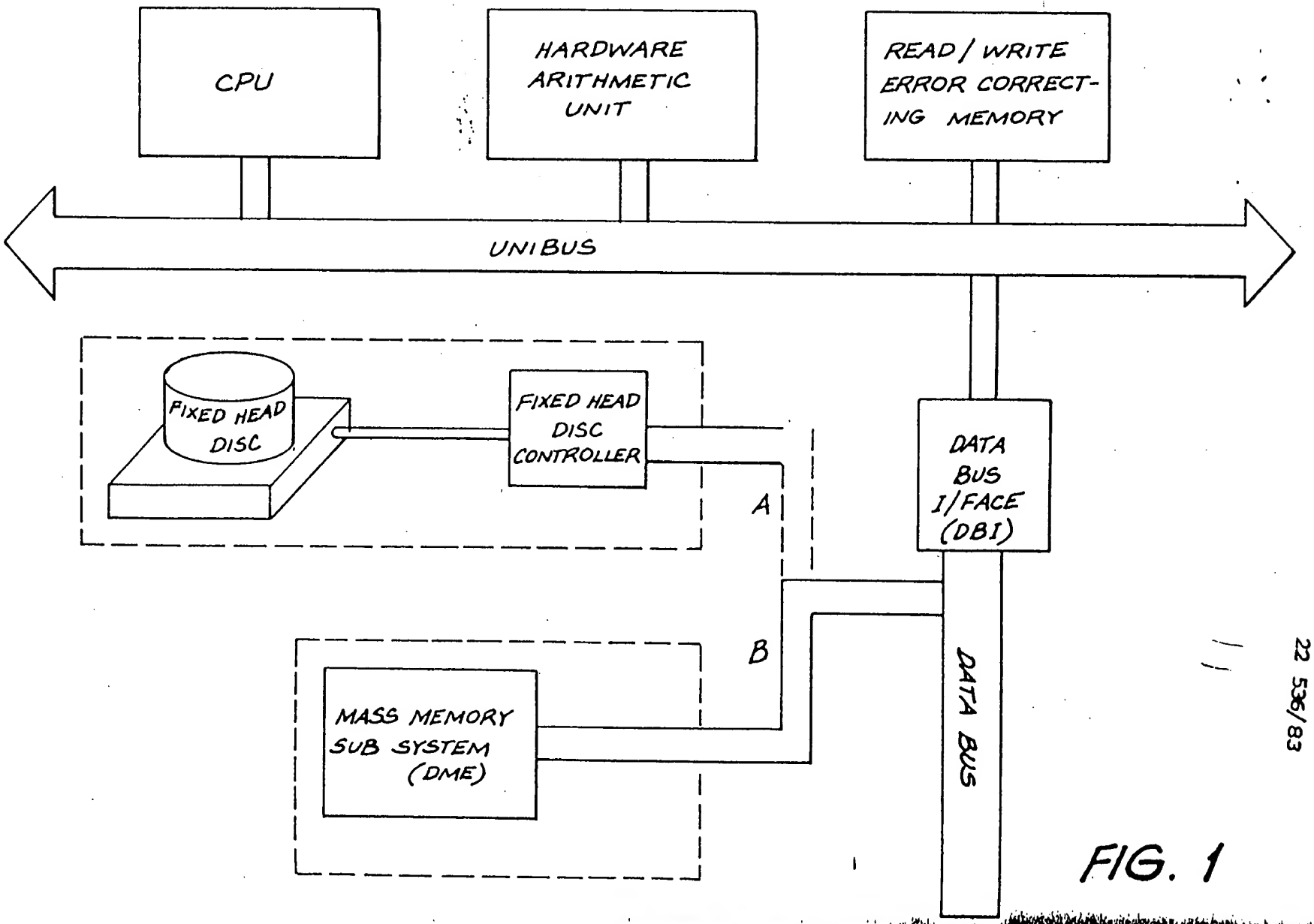
1. A solid state memory system for emulating a rotating magnetic memory device, said memory system comprising electronic controls means adapted to be connected to a host computer, and a semi-conductor memory connected to said electronic control means, said electronic control menas having circuit means for translating address signals from said host computer for the magnetic memory device to corresponding address signals for said semi-conductor memory, wherein no modifictions are required to said host computer when said solid state memory system replaces said rotating magnetic device.

2. A memory system as claimed in claim 1 wherein said address signals for the magnetic memory device include starting track and block address, and number of blocks to be transferred, said circuit means being hard wired to convert the starting track and block address signals into address signals for said semi-conductory memory.

3. A memory system as claimed in claim 2 wherein said semi-conductor memory address signals are multiplexed in time.

4. A memory system as claimed in any one of claims 1 to 3, further comprising a microprocessor connected to said electronic control means for accessing the contents of said semi-conductor memory and testing said electronic control means.

5. A memory system as claimed in any one of claims 1 to 4, further comprising display means connected to



22 536/83

FIG. 1

said electronic control means, said display means having a display panel for indicating current address and operational status information.

6. A memory system as claimed in any preceding claim, wherein said semi-conductor memory comprises dynamic RAM integrated circuits.

7. A memory system as claimed in claim 6 wherein said RAM integrated circuits are housed on at least one circuit board, and said electronic control means are housed on at least one circuit board, said board(s) being connected to a common backplane.

8. A memory system as claimed in claim 6 or 7, further comprising means for refreshing the contents of said dynamic RAM integrated circuits.

9. A memory system as claimed in claim 2, wherein said electronic control means includes parity generating means for generating check bits from data bits transferred between said host computer and said semi-conductor memory.

10. A solid state memory system for emulating a rotating magnetic memory device, said memory system being substantially as described herein with reference to the accompanying drawings.

DATED this THIRD day of NOVEMBER, 1986

BLUE CIRCLE SOUTHERN CEMENT LIMITED

Patent Attorneys for the Applicant
SPRUSON & FERGUSON

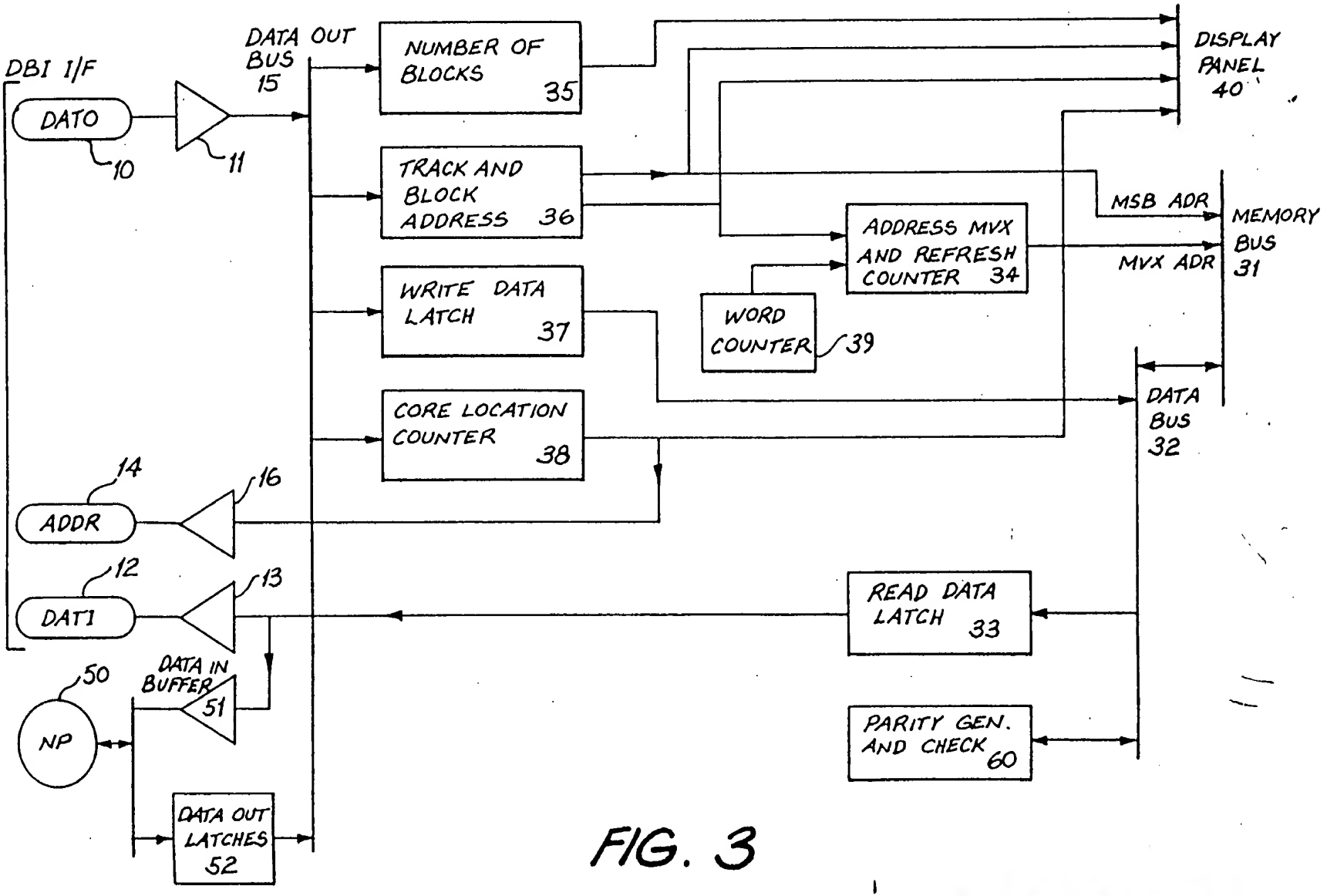

DBI I/F
DATO
10
11
DATA OUT BUS 15
NUMBER OF BLOCKS 35
TRACK AND BLOCK ADDRESS 36
WRITE DATA LATCH 37
CORE LOCATION COUNTER 38
WORD COUNTER 39
ADDRESS MVX AND REFRESH COUNTER 34
DISPLAY PANEL 40
MSB ADR
MVX ADR
MEMORY BUS 31
DATA BUS 32
READ DATA LATCH 33
PARITY GEN. AND CHECK 60
14
ADDR
16
12
DATI
13
50
NP
DATA IN BUFFER 51
DATA OUT LATCHES 52

FIG. 3

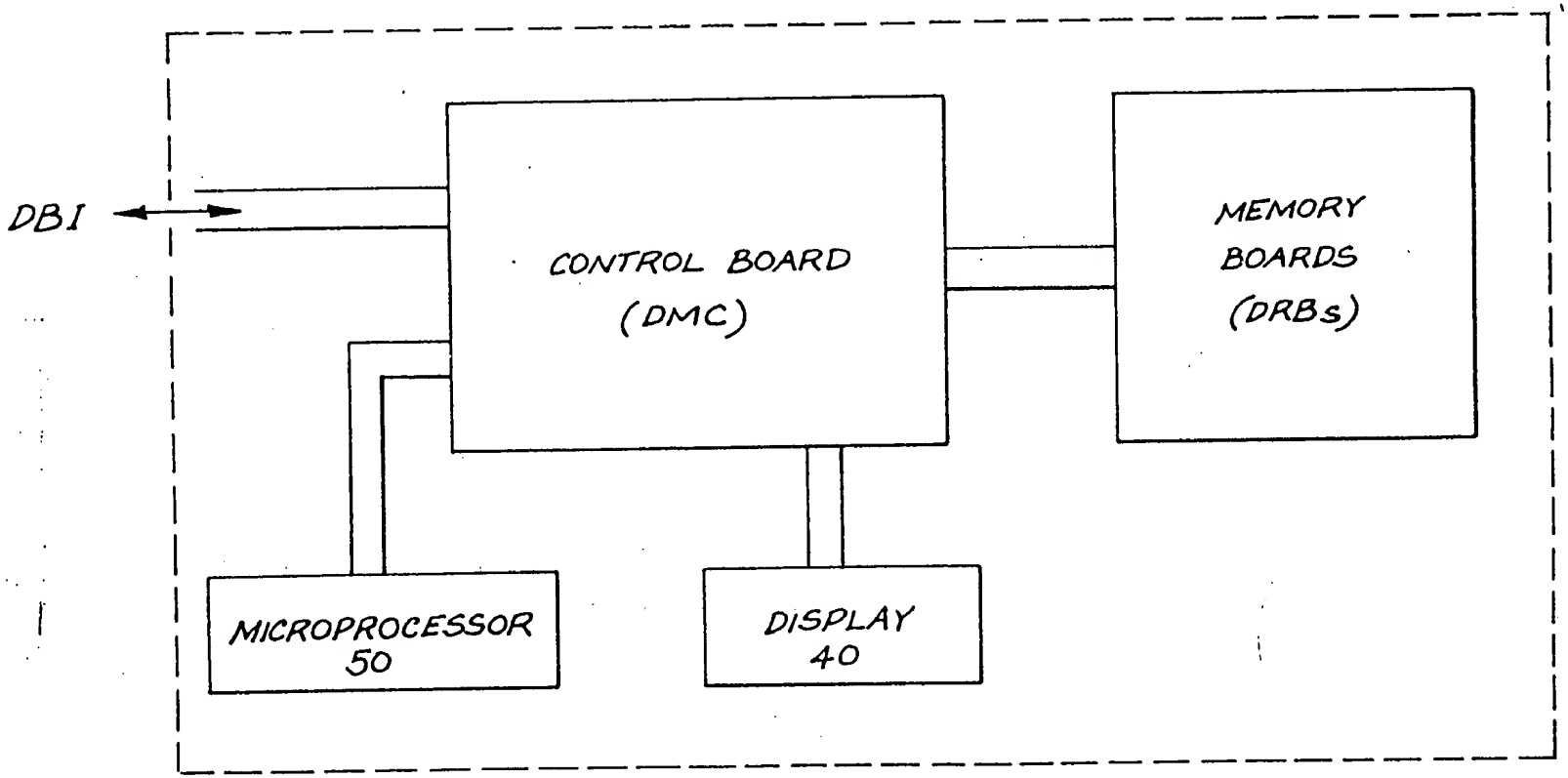

DBI
CONTROL BOARD
(DMC)
MEMORY
BOARDS
(DRBs)
MICROPROCESSOR
50
DISPLAY
40

FIG. 2

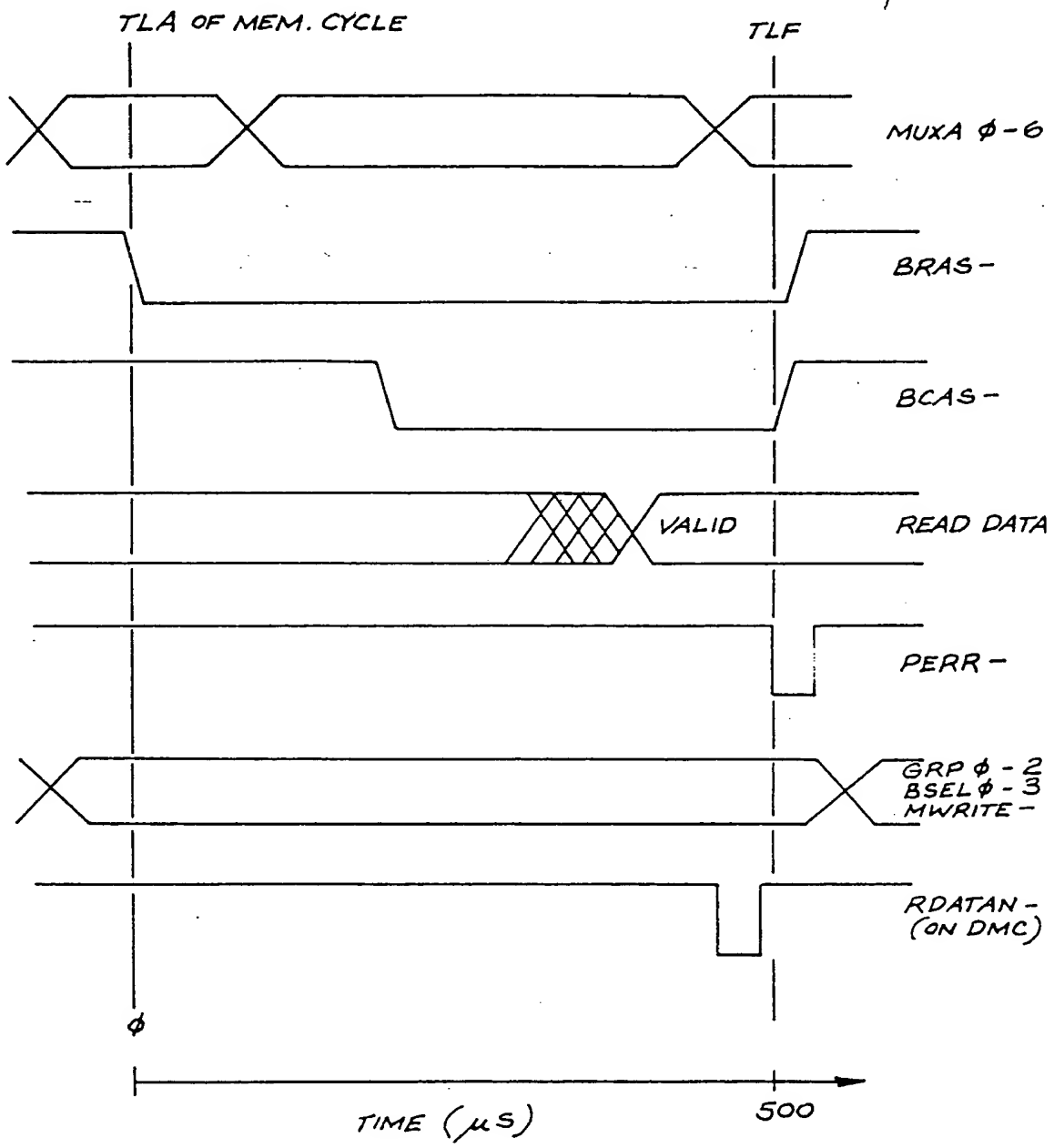

TLA OF MEM. CYCLE
TLF
MUXA ϕ-6
BRAS-
BCAS-
VALID
READ DATA
PERR-
GRP ϕ-2
BSEL ϕ-3
MWRITE-
RDATAN-
(ON DMC)
ϕ
TIME (μS)
500

FIG. 5

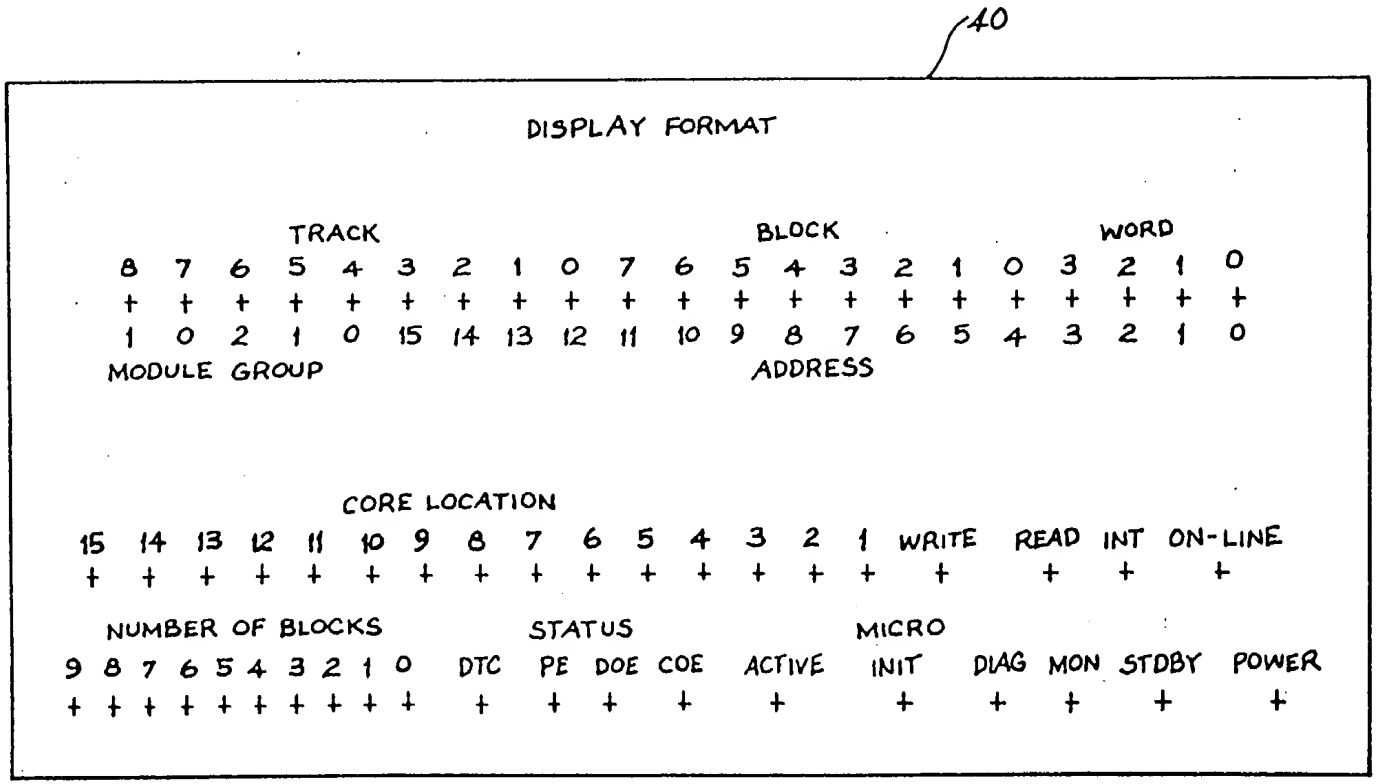

40
DISPLAY FORMAT
TRACK
BLOCK
WORD
8 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 3 2 1 0
1 0 2 1 0 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MODULE GROUP
ADDRESS
CORE LOCATION
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 WRITE READ INT ON-LINE
NUMBER OF BLOCKS
STATUS
MICRO
9 8 7 6 5 4 3 2 1 0 DTC PE DOE COE ACTIVE INIT DIAG MON STDBY POWER

FIG. 4

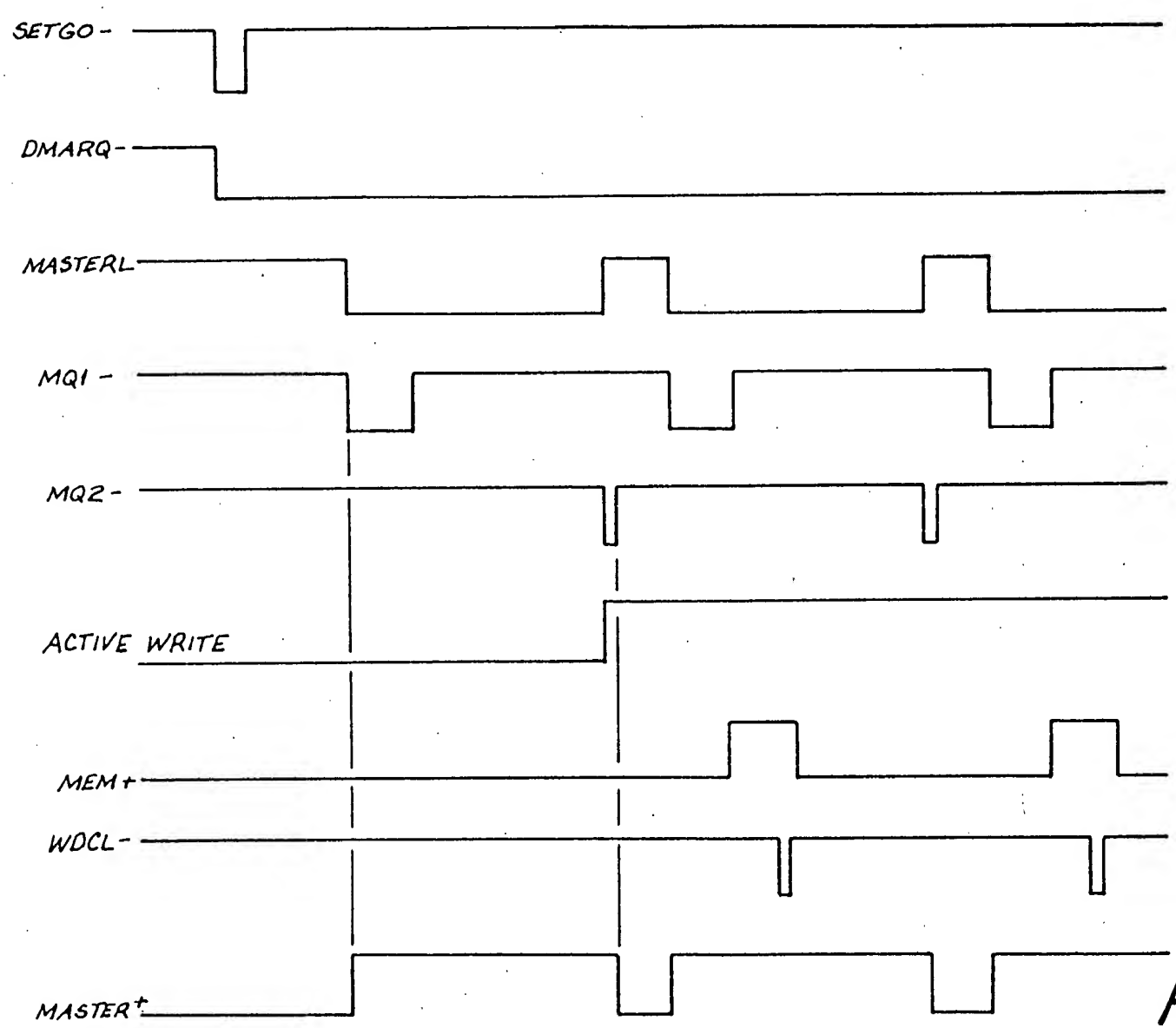


FIG. 6

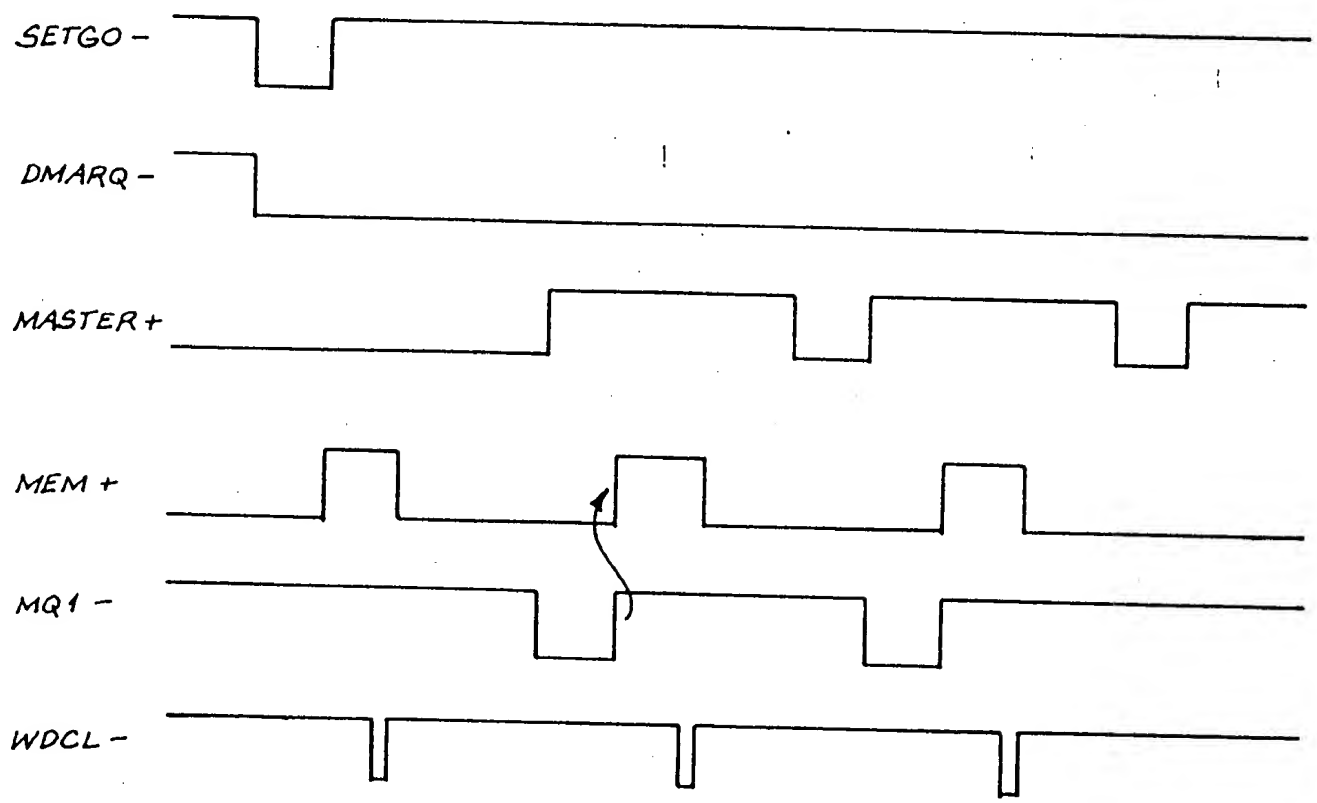


FIG. 7

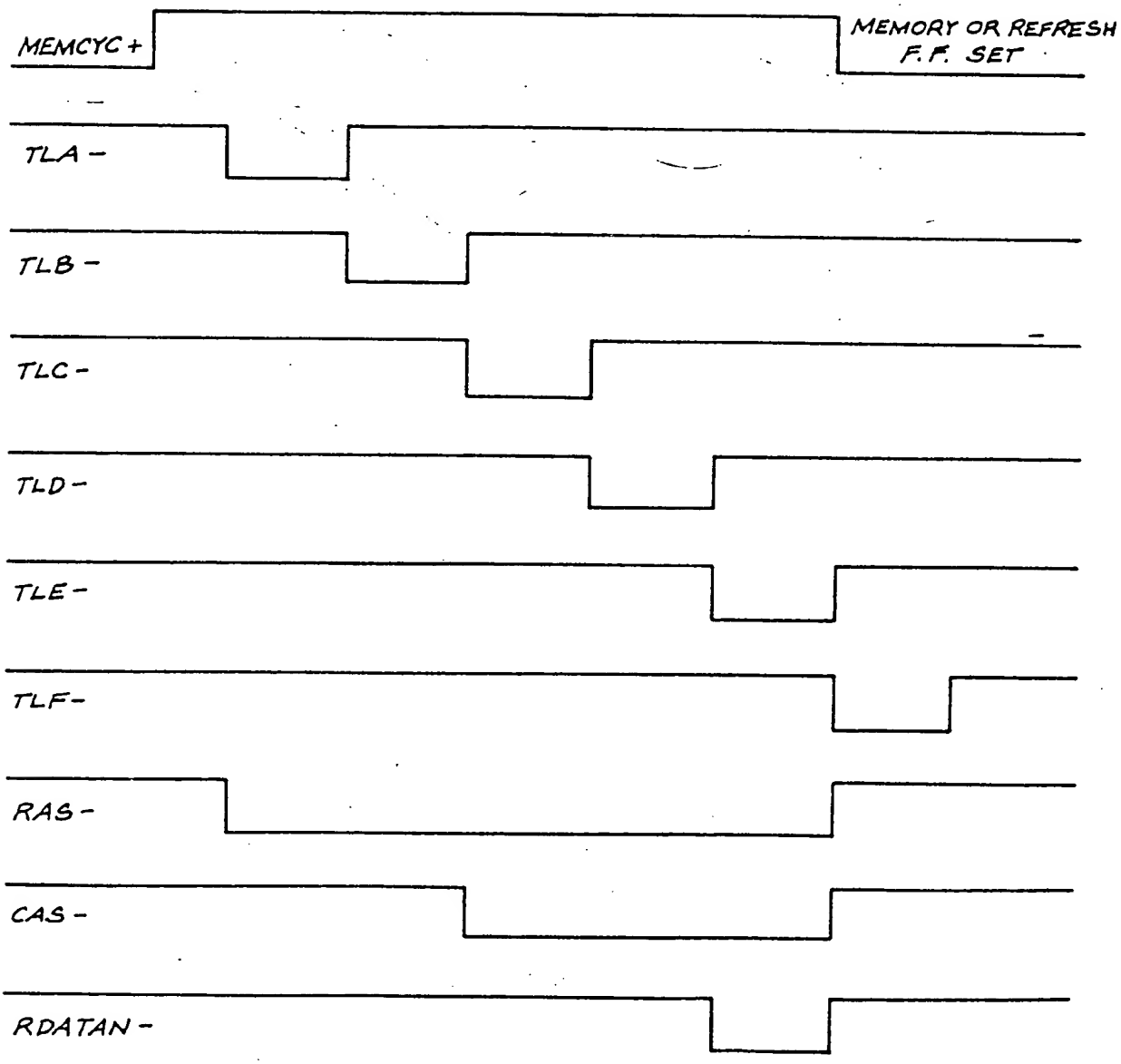

MEMCYC +
MEMORY OR REFRESH F.F. SET
TLA -
TLB -
TLC -
TLD -
TLE -
TLF -
RAS -
CAS -
RDATAN -

FIG. 8